International Journal of Technology and Engineering System(IJTES)
ISSN: 0976-1345
Vol5.No.2 2013 pp 1-7
available at: www.ijcns.com
Paper Received :15-05-2013
Paper Accepted:08-06-2013
Paper Reviewed by: 1. Prof. Premananda Reddy 2.Dr.R. Umarani
Editor : Prof. P.Muthukumar

A STEP-DOWN AND STEP-UP DC-DC VOLTAGE CONVERTER COMBINING KY AND SR BUCK CONVERTERS

P.Pugazhendiran[1], Dr.J.Baskaran[2] R.Vinothini,[3]
[1,3]IFET College of Engineering, Villupuram.
[2]Adhiparasakthi college of Engineering, Melmaruvathur.
pugazhifet@gmail.com, baski11@gmail.com vinothinieeeifet@gmail.com

***Abstract*—In this paper, a step-down and step-up Dc-Dc converter, i.e., a buck–boost converter, with a positive output voltage, is presented, which combines the KY converter and the traditional synchronously rectified (SR) buck converter. By doing so, the problem in voltage bucking of the KY converter can be solved, thereby increasing the application capability of the KY converter. Since such a converter operates in continuous conduction mode inherently, it possesses the non-pulsating output current, thereby not only decreasing the current stress on the output capacitor but also reducing the output voltage ripple. Above all, both the KY converter and the SR buck converter, combined into a buck–boost converter with no right-half plane zero, use the same power switches, thereby causing the required circuit to be compact and the corresponding cost to be down. Furthermore, during the energization period, the input voltage of the KY converter comes from the input voltage source, whereas during the de-energization period, the input voltage of the KY converter comes from the output voltage of the SR buck converter.**

***Index Terms*—Buck–boost converter, KY converter, right-half plane zero, synchronously rectified (SR) buck converter.**

1.INTRODUCTION

As generally recognized, many applications require voltage-bucking/boosting converters, such as portable devices, car electronic devices, etc. This is because the battery has quite large variations in output voltage, and hence, the additional switching power supply is indispensable for processing the varied input voltage so as to generate the stabilized output voltage. There are several types of non-isolated voltage buck/ boosting converter [1]–[9], such as buck–boost converter, single-ended primary-inductor converter (SEPIC), Cuk converter, Zeta converter, Luo converter and its derivatives, etc. However, these converters, operating in the continuous conduction mode (CCM), possess right-half plane zeros, thus causing system stability to be low. Consequently, a KY buck–boost converter [10] has been presented to conquer the aforementioned problems, but it has a serious problem in four power switches used, thereby causing the corresponding cost to be up.

In order to reduce the number of power switches in [10], the KY converter and the SR buck converter, combined into a buck–boost converter, i.e., 2D converter, both use the same power switches. Aside from this, the proposed converter has no right-half plane zero due to the input connected to the output during the turn-on period, and this converter always operates in CCM due to the positive and negative inductor currents existing at light load simultaneously. As compared with the converters previously stated, this converter has the nonpulsating output inductor current, thereby causing the current stress on the output capacitor to be decreased, and hence, the corresponding output voltage ripple to be small. Moreover, such a converter has the positive output voltage different from the negative output voltage of the traditional buck–boost converter. In this letter, the detailed illustration of the operation of this converter is given, along with some experimental results provided to verify the effectiveness of the proposed topology.

Prior to the end of this section, there is a comparison between the converters presented in [11] and the proposed converter. Since the proposed converter is used to buck/boost voltage, the voltage boosting range is not so high, that is, the voltages across two energy-transferring capacitors C_1 and C_2 are both D times the input voltage, where D is the duty cycle of the gate driving signal for the main switch. Regarding the converters shown in [11], the voltages across two energy-transferring capacitors C_{1a} and C_{1b} for the hybrid Cuk converter, the hybrid Zeta converter, and the hybrid SEPIC converter are $1/(1-D)$, $D/(1-D)$, and $1/(1-D)$ times the input voltage, respectively. Therefore, the converters shown in [11] have higher voltage conversion ratios than that of the proposed converter. Therefore, from an industrial point of view, the converters shown in [11] are suitable for sustainable energy applications, whereas the proposed converter is suitable for portable products.

Furthermore, since the proposed converter comes from the KY converter, the detailed comparisons

International Journal of Technology and Engineering System(IJTES)
ISSN: 0976-1345
Vol5.No.2 2013 pp 1-7
available at: www.ijcns.com
Paper Received :15-05-2013
Paper Accepted:08-06-2013
Paper Reviewed by: 1. Prof. Premananda Reddy 2.Dr.R. Umarani
Editor : Prof. P.Muthukumar

between the proposed buck–boost converter and the KY converter are described as follows.

1) Both converters always operate in CCM. That is, the negative current can be allowed at light load, but the corresponding average current must be positive.
2) Both converters have individual output inductors, thereby causing the output currents to be nonpulsating.
3) The proposed converter has one additional inductor and one additional capacitor so as to execute voltage bucking/ boosting as compared with the KY converter. Therefore, the proposed converter has the voltage conversion ratio of 2D, and hence possesses voltage bucking with the duty cycle locating between 0 and 0.5 and voltage boosting with the duty cycle locating between 0.5 and 1. On the other hand, the KY converter has the voltage conversion ratio of 1 + D, and hence only possesses voltage boosting with the duty cycle locating between 0 and 1. In addition, the maximum voltage conversion ratios for both are identical, equal to 2.
4) Both these converters can operate bidirectionally. The proposed converter works with the backward voltage conversion ratio of $0.5/(1-D)$, whereas the KY converter works with the backward voltage conversion ratio of $1/(2-D)$.

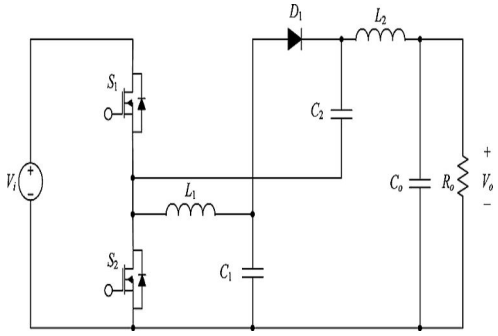

Fig. 1. Proposed buck–boost converter.

2.PROPOSED CONVERTER STRUCTURE

Fig. 1 shows a novel buck–boost converter, which combines two converters using the same power switches. One is the SR buck converter, which is built up by two power switches S_1 and S_2 , one inductor L_1 , one energy transferring capacitor C_1 , whereas the other is the KY converter, which is constructed by two power switches S_1 and S_2 , one power diode D_1 which is disconnected from the input voltage source and connected to the output of the SR buck converter, one energy-transferring capacitor C_2 , one output inductor L_2 , and one output capacitor C_o. The output load is signified by R_o . Furthermore, during the magnetization period, the input voltage of the KY converter comes from the input voltage source, whereas during the demagnetization period, the input voltage of the KY converter comes from the output voltage of the SR buck converter.

In addition, during the startup periodwith S_1 beingONand S_2 being OFF, L_1 and L_2 are both magnetized. At the same time, C_1 is charged, and hence, the voltage across C_1 is positive, whereas C_2 is reverse charged, and hence, the voltage across C_2 is negative. Sequentially, during the startup period with S_1 being OFF and S_2 being ON, L_1 and L_2 are both demagnetized. At the same time, C_1 is discharged. Since C_2 is connected in parallel with C_1 , C_2 is reverse charged with the voltage across C_2 being from negative to positive, and finally, the voltage across C_2 is the same as the voltage across C_1 . After this time onward, the working behavior of this converter will follow the timing sequence shown in Fig. 2.

3.BASIC OPERATING PRINCIPLES

Before this section is taken up, there are some assumptions and symbols that are given as follows: 1) all the components are ideal; 2) the blanking times between S_1 and S_2 are omitted; 3) the voltage drops across the switches and diode during the turn-on period are negligible; 4) the values of C_1 and C_2 are large enough to keep V_{C1} and V_{C2} almost constant, that is, variations in V_{C1} and V_{C1} are quite small during the charging and discharging period; 5) the dc input voltage is signified by V_i , the dc output voltage is represented by V_o , the dc output current is expressed by I_o , the gate driving signals for S_1 and S_2 are indicated byM_1 andM_2 , respectively, the voltages on S_1 and S_2 are represented by v_{S1} and v_{S2} , respectively, the voltages on L_1 and L_2 are denoted by v_{L1} and v_{L2} , respectively, the currents in L_1 and L_2 are signified by i_{L1} and i_{L2} , respectively, and the input current is expressed by i_i ; and 6) the currents flowing through L_1 and L_2 are both positive. Since this converter always operates in CCM inherently, the turn-on type is $(D, 1-D)$, where D is the duty cycle of the gate driving signal for S_1 and $1-D$ is the duty cycle of the

International Journal of Technology and Engineering System(IJTES)
ISSN: 0976-1345
Vol5.No.2 2013 pp 1-7
available at: www.ijcns.com
Paper Received :15-05-2013
Paper Accepted:08-06-2013
Paper Reviewed by: 1. Prof. Premananda Reddy 2.Dr.R. Umarani
Editor : Prof. P.Muthukumar

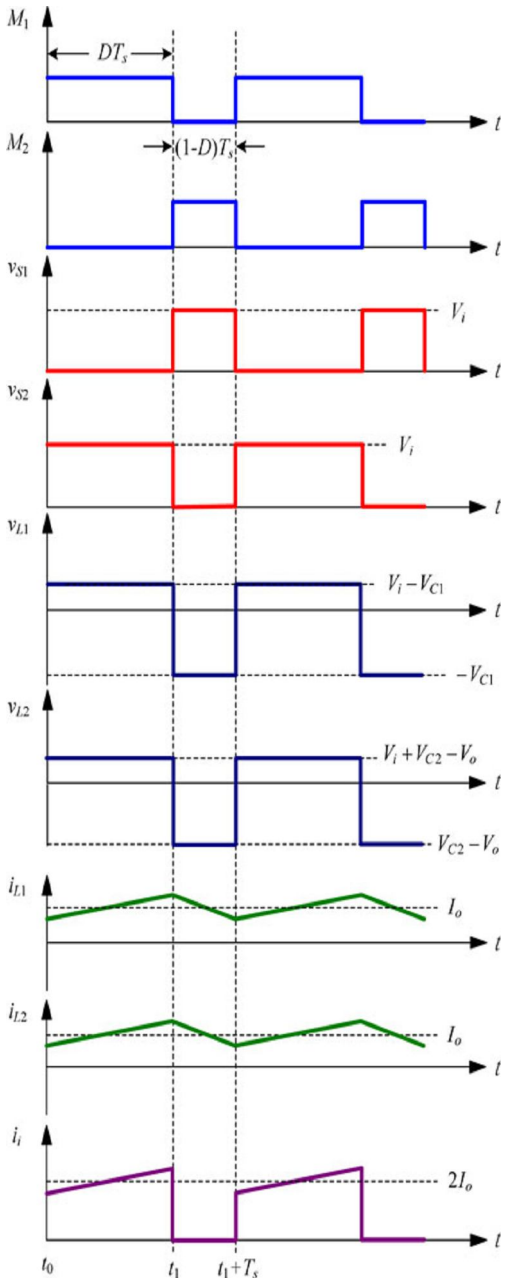

Fig. 2. Key waveforms of the proposed converter

gate driving signal for S_2 . Fig. 2 shows the key waveforms of the proposed converter with a switching period of T_s under i_{L1} and i_{L2} being positive for any time. It is noted that from Fig. 2, the voltage stresses for S_1 and S_2 are both identical and equal to the input voltage, and the input current waveform is pulsating. In the following, there are two operating states to be described.

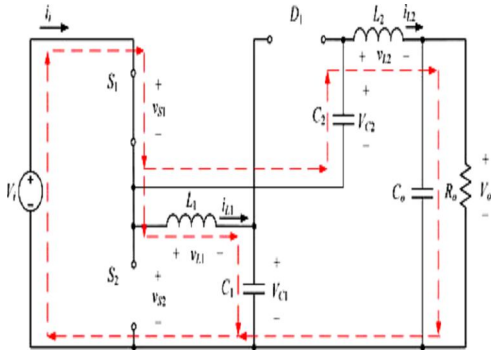

Fig. 3. Current flow in state 1.

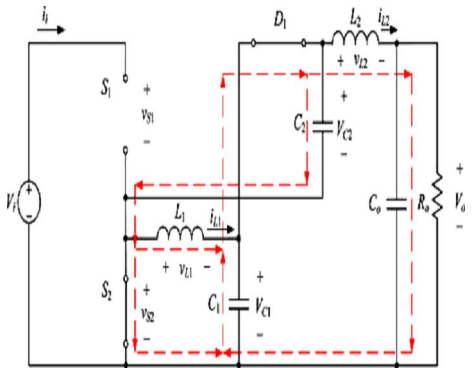

Fig. 4. Current flow in state 2.

State 1: As shown in Fig. 3, S_1 is turned ON but S_2 is turned OFF. During this state, the input voltage provides energy for L_1 and C_1 . Hence, the voltage across L_1 is V_i minus V_{C1} , thereby causing L_1 to be magnetized, and C_1 is charged. At the same time, the input voltage, together with C_2 , provides the energy for L_2 and the output. Hence, the voltage across L_2 is V_i plus V_{C2} minus V_o , thereby causing L_2 to be magnetized, and C_2 is discharged. Therefore, the related equations are depicted as follows:

$$v_{L1} = V_i - V_{C1} \quad (1)$$

$$v_{L2} = V_i + V_{C2} - V_o . \quad (2)$$

International Journal of Technology and Engineering System(IJTES)
ISSN: 0976-1345
Vol5.No.2 2013 pp 1-7
available at: www.ijcns.com
Paper Received :15-05-2013
Paper Accepted:08-06-2013
Paper Reviewed by: 1. Prof. Premananda Reddy 2.Dr.R. Umarani
Editor : Prof. P.Muthukumar

State 2: As shown in Fig. 4, S_1 is turned OFF but S_2 is turned ON. During this state, the energy stored in L_1 and C_1 is released to C_2 and the output via L_2 . Hence, the voltage across L_1 is minus V_{C1} , thereby causing L_1 to be demagnetized, and C_1 is discharged. At the same time, the voltage across L_2 is V_{C2} minus V_o , thereby causing L_2 to be demagnetized, and C_2 is charged. Therefore, the associated equations are described as follows:

$$v_{L1} = -V_{C1} \quad (3)$$

$$v_{L2} = V_{C2} - V_o \quad (4)$$

$$V_{C2} = V_{C1} \quad (5)$$

By applying the voltage-second balance to (1) and (3), the following equation can be obtained as

$$(Vi - VC1)\, D\, Ts + (-VC1)\,(1-D)\, Ts = 0 \quad (6)$$

Therefore, by simplifying (6), the following equation can be obtained as

$$VC1 = D \,.\, Vi \,. \quad (7)$$

Consecutively, by applying the voltage-second balance to (2) and (4), the following equation can be obtained as

$$(V_i + V_{C2} - V_o)\, D\, T_s + (V_{C2} - V_o)(1 - D)\, T_s = 0. \quad (8)$$

Hence, by substituting (5) and (7) into (8), the voltage conversion ratio of the proposed converter can be obtained as

$$\frac{Vo}{Vi} = 2D \quad (9)$$

Therefore, such a converter can operate in the buck mode as the duty cycle D is smaller than 0.5, whereas it can operate in the boost mode as D is larger than 0.5. In addition, based on (5), (7), and (9), the dc voltages across C_1 and C_2 can be expressed to be

$$VC1 = VC2 = 0.5Vo \,. \quad (10)$$

KEY DESIGN PARAMETER CONSIDERATIONS

In this section, the design of inductors and capacitors are mainly taken into account.

A. Inductor Design

From an industrial point of view, the inductor is designed under the condition that no negative current in the inductor exists above 25% of the rated dc load current. Therefore, in this letter, the critical point between positive current and negative current in the inductor is assumed at 25% of the rated dc load current. Therefore, the peak-to-peak values of i_{L1} and i_{L2} are expressed by Δi_{L1} and Δi_{L2}, respectively, and can be obtained according to the following equation:

$$\Delta iL1 = \Delta iL2 = 0.5 Io_{\_rated} \,. \quad (11)$$

Therefore, Δi_{L1} and Δi_{L2} are 1.5 A. Since the high input voltage makes the inductor not easier to escape from the negative current than the low input voltage, the inductor design is mainly determined by the high input voltage, namely, 16V. Hence, the corresponding minimum duty cycle D_{min} is 0.375. Moreover, based on (10), V_{C1} and V_{C2} are both 0.5 V_o, namely, 6V. Also, the values of L_1 and L_2 can be obtained according to the following equations:

$$L1 \geq Dmin. \frac{(Vi - Vc1)}{(\Delta iL1.fs)} \quad (12)$$

$$L2 \geq Dmin. \frac{(Vi + Vc2 - Vo)}{(\Delta iL2.fs)} \quad (13)$$

Therefore, the values of L_1 and L_2 both are calculated to be not less than 12.5 μH, and finally, L_1 and L_2 have individual PC47RM5Z ferrite cores with turns of 10.5, corresponding to 14 μH.

B. Capacitor Design

1) Output Capacitor Design:

Prior to designing C_o, it is assumed that the output voltage ripple Δv_o is smaller than 1% of the dc output voltage, that is, Δv_o is smaller than 120 mV. Hence, the equivalent series resistance of the output capacitor.ESR can be represented by

$$ESR \leq \frac{\Delta Vo}{\Delta iL2} \quad (14)$$

For that reason, ESR is calculated to be smaller than 80 mΩ, and finally, one Nippon Chemi-Con (NCC) KY series capacitor of 470 μF with ESR equal to 46 mΩ is chosen for C_o.

2) *Energy-Transferring Capacitor Design:*

International Journal of Technology and Engineering System(IJTES)
ISSN: 0976-1345
Vol5.No.2 2013 pp 1-7
available at: www.ijcns.com
Paper Received :15-05-2013
Paper Accepted:08-06-2013
Paper Reviewed by: 1. Prof. Premananda Reddy 2.Dr.R. Umarani
Editor : Prof. P.Muthukumar

Prior to designing the energy-transferring capacitors C_1 and C_2, it is assumed that the values of C_1 and C_2 are large enough to keep V_{C1} and V_{C2}, almost at 6V, and hence, variations in V_{C1} and V_{C2} are somewhat small and are defined to be ΔV_{C1} and ΔV_{C2}, respectively. Based on this assumption, ΔV_{C1} and ΔV_{C2} are both set to smaller than 1% of $V_{C\,1}$ and $V_{C\,2}$, respectively, namely, both are smaller than 60 mV. Also, in State 1, C_1 is charged whereas C_2 is discharged. Therefore, the values of C_1 and C_2 must satisfy the following equations:

$$C1 \geq \frac{(Io_{rated} . Dmax)}{(\Delta Vc1 . fs)} \qquad (15)$$

$$C2 \geq \frac{(Io_{rated} . Dmax)}{(\Delta Vc1 . fs)} \qquad (16)$$

Since the maximum duty cycle D_{max} occurs at the input voltage of 10V, namely, 0.6, both the values of C_1 and C_2 are not less than 150 μF. Finally, C_1 and C_2 have individual NCC KY series capacitors of 470 μF.

4.SIMULATION RESULTS

The simulation result for the proposed step-up and step-down dc-dc converter is explained below. In this, fig.6 shows the simulation circuit for proposed converter in open loop condition under a resistive load. Here, by taking 50V as the input voltage, with 60 percent duty cycle in boost mode, then the output voltage obtained here is nearly equal to 60V. By varying the duty cycle voltage bucking and voltage boosting operation can be performed. Thus the, simulation waveform for proposed converter in open loop condition under a load is shown in fig.7.

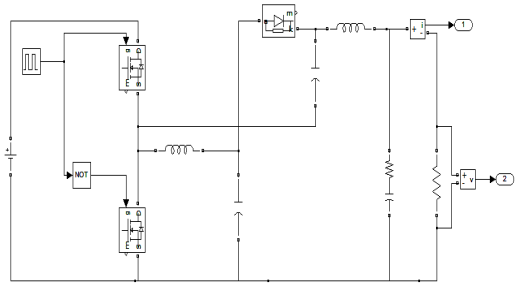

Fig.6. Open loop simulation circuit.

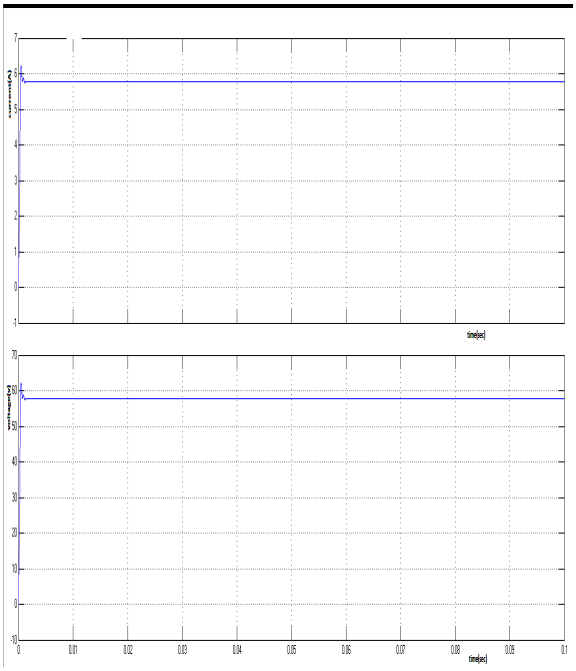

Fig.7. Simulation waveform for open loop proposed converter.

Fig.8 shows the closed loop simulation circuit for proposed converter. The controller which is used in this circuit is PID integral controller. In closed loop circuit, with respect to the reference voltage, the voltage step-up and step-down operation can be performed. Here the pulse width modulation block is used to provide a proper pulse to the switches. The PID integral controller produces control signal based on the voltage error signal (difference between output load voltage and reference voltage) and thus the change in error signal is obtained from comparator output. Usually the PID controller is used to convert the non-steady state response signal into steady state response signal. According to the reference voltage the duty ratio of the pulse width modulation can be changed with the help of PID integral controller.

The PWM signal is fed as a switching signal to the MOSFET switches of the proposed converter and the output of converter can be varied by varying the duty cycle of the switching signal. Instead of PID controller, the Adapter Neuro Fuzzy controller can also be used for the closed loop proposed converter. According to the reference paper [18] i.e., Two stage KY converter the ANFIS acts as a controller circuit for robust control of converter.

International Journal of Technology and Engineering System(IJTES)
ISSN: 0976-1345
Vol5.No.2 2013 pp 1-7
available at: www.ijcns.com
Paper Received :15-05-2013
Paper Accepted:08-06-2013
Paper Reviewed by: 1. Prof. Premananda Reddy 2.Dr.R. Umarani
Editor : Prof. P.Muthukumar

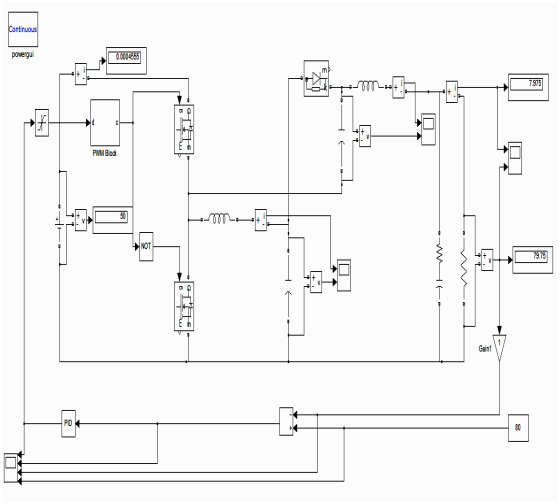

Fig. 8. Closed loop simulation circuit

Fig. 9 and fig. 10 shows the current waveform for inductive parameter i.e., iL1 & iL2 and the voltage waveform for capacitive parameter i.e., Vc1 & Vc2 in a proposed converter. At the end of the simulation result, the output current and voltage waveform with respect to time in seconds for closed loop proposed converter by using the PID integral controller are shown in fig.11. the voltage bucking and boosting operation of closed loop proposed converter can be modified by changing the reference voltage. Hence the duty cycle of the PWM block may automatically changed according to the reference voltage.

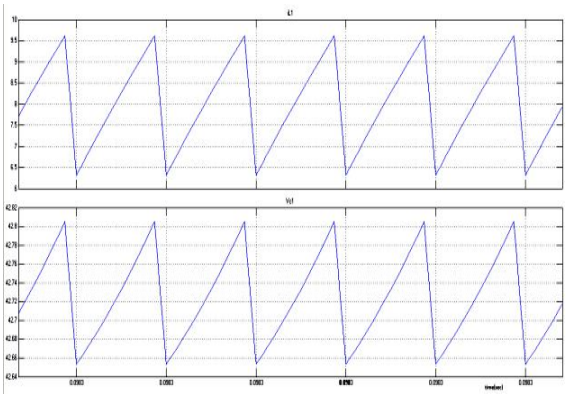

Fig .9 .Waveform for current through inductance L_1 and voltage across capacitor C_1.

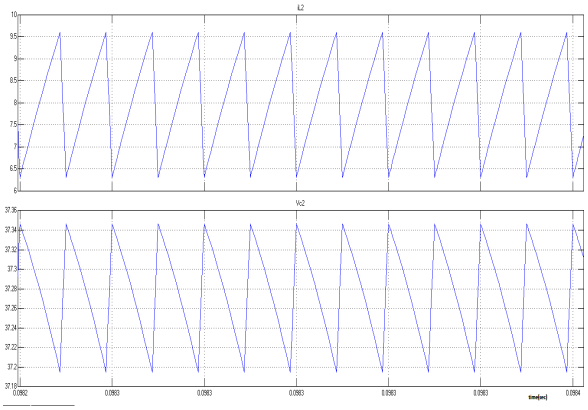

Fig . 10. Waveform for inductive current L2 and voltage across capacitor C2.

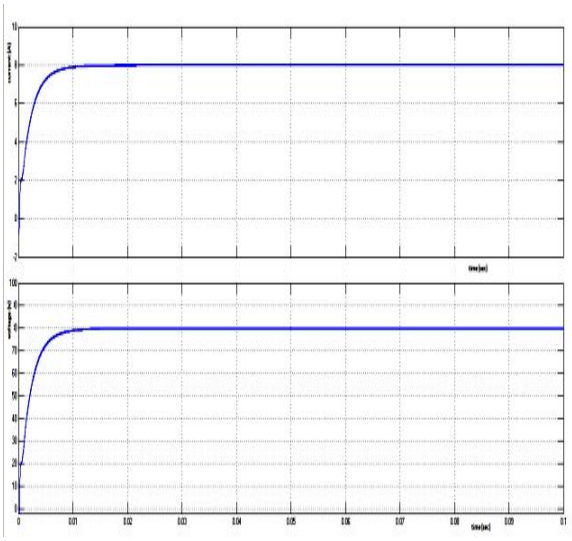

Fig.11.Waveform for output current for closed loop proposed converter.

5. CONCLUSION

The proposed step-down and step-up dc-dc converter, combining the KY converter and the established SR buck by using the same power switches, has a positive output voltage and no right-half plane zero. Additionally, this converter always operates in CCM essentially ,thus causing variations in duty cycle all over the load range not to be so much, and hence, the control of the converter to be uncomplicated. Above all, such a converter possesses the non-pulsating output current, in this manner, not only decreasing the current stress on the output capacitor but also reducing the

International Journal of Technology and Engineering System(IJTES)
ISSN: 0976-1345
Vol5.No.2 2013 pp 1-7
available at: www.ijcns.com
Paper Received :15-05-2013
Paper Accepted:08-06-2013
Paper Reviewed by: 1. Prof. Premananda Reddy 2.Dr.R. Umarani
Editor : Prof. P.Muthukumar

output voltage ripple. By means of both open-loop and closed-loop simulation results, it can be seen that for any dc input voltage, the proposed converter can stably work for both voltage bucking and voltage boosting efficiently. Hence, the proposed dc-dc KY boost and SR buck converter can be used for portable applications such as car electronic devices.

REFERENCES

[1] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA, Kluwer, 2001.

[2] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics*, 2nd ed. New York: Willey, 2003.

[3] F. L. Luo, "Positive output Luo converters: Voltage lift technique," *IEEE Proc. Elect. Power Appl.*, vol. 4, no. 146, pp. 415–432, Jul. 1999.

[4] X. Chen, F. L. Luo, and H. Ye, "Modified positive output Luo converter," in *Proc. IEEE Int. Conf. Power Electron. Drive Syst.*, 1999, pp. 450–455.

[5] F. L. Luo and H. Ye, "Positive output super-lift converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 105–113, Jan. 2003.

[6] F. L. Luo and H. Ye, "Positive output multiple-lift push-pull switchedcapacitorLuo-converters," *IEEE Trans. Ind. Electron.*, vol. 51, no.3, pp. 594–602, Jun. 2004.

[7] M. Zhu and F. L. Luo, "Development of voltage lift technique on doubleoutputtransformerless DC–DC converter," in *Proc. 33rd Annu Conf. Ind. Electron. Soc.*, 2007, pp. 1983–1988.

[8] M. Zhu and L. Luo, "Implementing of developed voltage lift technique on SEPIC, Cuk and double-output DC–DC converters," in *Proc. IEEE Int. Conf. Ind. Electron.*, 2007, pp. 674–681.

[9] K. Viswanathan, D. Srinivasan, and R. Oruganti, "A universal fuzzy controllerfor a non-linear power electronic converter," in *Proc. IEEE Int.Conf. Fuzzy Syst.*, 2002, pp. 46–51.

[10] K. I. Hwu and Y. T. Yau, "Two types of KY buck–boost converters," *IEEETrans. Ind. Electron.*, vol. 56, no. 8, pp. 2970–2980, Aug. 2009.

[11] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Hybrid switched-capacitor Cuk/Zeta/Sepic converters in step-up mode," *Proc. IEEE Int. Symp. Circuits Syst.*, pp. 1310–1313, 2005.

BIOGRAPY

P.Pugazhendiran was born in Tamilnadu, in 1979. Received his UG degree in Electrical and Electronics Engineering from Coimbatore Institute of Technology (CIT) in 2001 and PG degree from College of Engineering Guindy (CEG), Anna University, Chennai in 2009. His research interest includes Power quality issues, Power Converters, Renewable energy sources, Electrical Drives. He Published More than 5 Engineering Books. Teaching Experience over a decade. He is currently working at I.F.E.T College of Engineering as Associate Professor and head of the department. He is a life member of ISTE

Prof. Dr. J. Baskaran was born in Tamilnadu. He received the Ph.D. degree from the Department of Electrical Engineering, he was an Professor /Head in the Department of Electrical and Electronics Engineering, Adhiparasakthi college of Engineering. His current research interests include power system engineering and power electronics.He published more than 20 National and International journals .He is the reviewer of M.Tech thesis evaluation member and also chairperson for national conference observer

R.Vinothini was born on 1992 at Villupuram, situated in Tamilnadu , at present he is pursuing her bachelor's degree in Electrical and Electronics Engineering department at IFET College of Engineering, Villupuram, Tamil Nadu. Her areas of interests are power electronics, Power quality issues and computer networks.